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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/669,769 | 09/23/2003 | Kenneth R. Smits | 42P11022C | 4381 |

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| EXAMINER | |
|---|---|
| INOA, MIDYS | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | |

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/669,769 | SMITS, KENNETH R. | |
| | Examiner | Art Unit | |
| | Midys Inoa | 2188 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/23/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. The drawings filed on September 23rd, 2003 have been accepted by the examiner.

### *Information Disclosure Statement*

2. The information disclosure statement (IDS) submitted on September 23rd, 2004 has been considered by the examiner.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 7, 9, and 12-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Kronstadt et al. (4,725,945).

Regarding Claim 1, Kronstadt teaches a memory 12 (Figure 4) comprising: a plurality of arrays of memory cells (memory banks 1- n), the arrays being arranged in banks, each bank including regular arrays (array of static column mode dynamic random access memories, Column 2, lines 11-28) and a redundant array (supports one or more redundant memory banks, Column 4, lines 25-45); a bus having sets of data lines for connection to the arrays; circuitry to connect (controller 18) a regular array to either a first set or a second set of the data lines (Figure 4, data lines $RAS_{1-n}$ and $CAS_{1-n}$), or to

disconnect the regular array from the bus. Memory controller 18 controls the data lines connecting to the different memory banks (Column 3, lines 9-20).

Regarding Claims 7 and 12, Kronstadt discloses a memory 12 (Figure 4), comprising: a plurality of arrays of memory cells, the arrays being arranged in banks (banks 1 – n), each bank including regular arrays (array of static column mode dynamic random access memories, Column 2, lines 11-28), A.sub.0-N, and a redundant array (supports one or more redundant memory banks, Column 4, lines 25-45); a data bus having sets of N sets of bus lines, B.sub.0-N, for connection to the arrays (Figure 4, data lines $RAS_{1-n}$ and $CAS_{1-n}$); logic associated with each array (controller 18), the logic being configured with a bit (valid field) that is set to a first state to connect an ith regular array to an ith set of the bus lines, with the redundant array being disconnected from the data bus; a change in the bit setting from the first state to a second state (identifies invalid banks) causing the regular array, A.sub.i, to be disconnected from the data bus and the redundant array to be connected to the data bus. In instances where invalid banks are identified prior to an access, the access of an invalid bank is avoided if possible. In this system, the invalid bank can be avoided by disabling the data line to such bank. In this case, the data line is not affected, but its connection to the invalid bank may be discontinued (Column 3, lines 15-45).

Regarding Claims 2 and 13, Kronstadt discloses the memory of claim 1 wherein the circuitry (controller 18) comprises a bit (valid field) that, when set to a first logic state (identifies invalid banks), causes the circuitry to disconnect the regular array from the bus. In instances where invalid banks are identified prior to an access, the access of an invalid bank is avoided if possible. In this system, the invalid bank can be avoided by

disabling the data line to such bank. In this case, the data line is not affected, but its connection to the invalid bank may be discontinued (Column 3, lines 15-45).

Regarding Claim 3, if the redundant bank is identified as a valid bank, such identification ("setting of the bit") can cause the controller to connect the redundant banks to a data line (See Figure 4).

Regarding Claims 4-5 and 9, the banks of Kronstadt et al. are arranged in a vertical linear configuration (See Figure 4) in which each banks is placed in one of multiple rows.

## *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 10 and 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Kronstadt et al. (4,725,945) in view of Parulkar (6,769,081)

Regarding Claims 10 and 14, Kronstadt teaches the invention of Claims 7 and 12 above. The controller of Kronstadt et al. has circuitry to set a bit in accordance to the validity of a bank. However, Kronstadt does not teach setting the conductivity of a fuse to change the status of a bit. Parulkar discloses a programmable fuse used to set an address bit (Column 4, lines 30-48). It would have been obvious to one of ordinary skill in the art at the time the invention was made to set the bit of Kronstadt in the same manner as that of Parulkar because fuses are commonly found as components in

computer systems and setting a fuse's conductivity is a quick and effective way to affect that value of a bit.

***Double Patenting***

7. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

8. Claims 1-15 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-3, 7-10, 13-14, 16, and 18-19 of U.S. Patent No.6,662,271. Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1-3 are anticipated by claims 1-3 of Patent 6,662,271; claim 4 is anticipated by claim 7 of Patent 6,662,271; claims 5 and 9 are anticipated by claim 8 of Patent 6,662,271; claims 6, 11, and 10 are anticipated by claim 9 of Patent 6,662,271; claim 7 is anticipated by claim 10 of Patent 6,662,271; claim 8 is anticipated by claim 14 of Patent 6,662,271; claim 10 is anticipated by claim 13 of Patent 6,662,271; claim 12 is anticipated by claim 16 of Patent 6,662,271; and claims 13-14 are anticipated by claims 18-19 of Patent 6,662,271. Although the some claims of Patent 6,662,27 have additional limitations, these claims still anticipate the claims of the

instant application because the instant claims are broader. Please refer to the explanation below.

With respect to claim 1, claim 1 of Patent 6,662,271 discloses the cache of the instant application. Please refer to the table below, illustrating the anticipatory relationship of the claims:

| **Instant Application** | **Patent 6,662,271** |
|---|---|
| A cache comprising: | A cache comprising: |
| a plurality of arrays of memory cells, | a plurality of arrays of memory cells, |
| the arrays being arranged in banks, each bank including regular arrays and a redundant array; | the arrays being arranged in banks, each bank including regular arrays and a redundant array; |
| a bus having sets of data lines for connection to the arrays; | a bus having sets of data lines for connection to the arrays, |
| | wherein each bank comprises N regular arrays and the bus comprises N sets of data lines; |
| circuitry to connect a regular array to either a first set or a second set of the data lines, or to disconnect the regular array from the bus. | and circuitry to connect a regular array to either a first set or a second set of the data lines, or to disconnect the regular array from the bus |

With respect to claim 2, claim 2 of Patent 6,662,271 is identical to claim 2 of the instant application.

With respect to claim 3, claim 3 of Patent 6,662,271 is identical to claim 3 of the instant application.

With respect to claim 4, claim 7 of Patent 6,662,271 is identical to claim 4 of the instant application.

With respect to claims 5 and 9, claim 8 of Patent 6,662,271 is identical to claims 5 and 9 of the instant application.

With respect to claims 6, 11, and 15, claim 9 of Patent 6,662,271 discloses the cache bank and repeaters of the instant application. Please refer to the table below, illustrating the anticipatory relationship of the claims:

| **Instant Application** | **Patent 6,662,271** |
|---|---|
| The cache of claim 2, further comprising: | A cache comprising: |
| | a plurality of arrays of memory cells, the arrays being arranged in banks, each bank including regular arrays and a redundant array; |
| | a bus having sets of data lines for connection to the arrays; |
| | circuitry to connect a regular array to either a first set or a second set of the data lines, or to disconnect the regular array from the bus; |
| a plurality of repeaters each of which provides for series connection of an array with a data line of the bus | and a plurality of repeaters each of which provides for series connection of an array with a data line of the bus. |

With respect to claim 7, claim 10 of Patent 6,662,271 discloses the cache of the instant application. Please refer to the table below, illustrating the anticipatory relationship of the claims:

| **Instant Application** | **Patent 6,662,271** |
|---|---|
| A cache, comprising: | A cache comprising: |
| a plurality of arrays of memory cells, the arrays being arranged in banks, each bank including regular arrays, A.sub.0-N, and a redundant array; | a plurality of arrays of memory cells, the arrays being arranged in banks, each bank including regular arrays, A.sub.0-N, and a redundant array; |
| a data bus having sets of N sets of bus lines, B.sub.0-N, for connection to the arrays; | a data bus having sets of N sets of bus lines, B.sub.0-N, for connection to the arrays; |
| logic associated with each array, the logic being configured with a bit that is set to a first state to connect an ith regular array to an ith set of the bus lines, with the redundant array being disconnected from the data bus; | logic associated with each array, the logic being configured with a bit that is set to a first state to connect an ith regular array to an ith set of the bus lines, with the redundant array being disconnected from the data bus; |
| a change in the bit setting from the first | a change in the bit setting from the first |

| | |
|---|---|
| state to a second state causing the regular array, A.sub.i, to be disconnected from the data bus and the redundant array to be connected to the data bus. | state to a second state causing the regular array, A.sub.i, to be disconnected from the data bus and the redundant array to be connected to the data bus, |
| | wherein the redundant array is connected to the Nth set of bus lines, B.sub.N, responsive to the change in the bit setting to the second state. |

With respect to claim 8, claims 14 and 7 of Patent 6,662,271 disclose the cache bank arrays of the instant application. Please refer to the table below, illustrating the anticipatory relationship of the claims:

| **Instant Application** | **Patent 6,662,271** |
|---|---|
| The cache of claim 7, | A cache comprising: . |
| wherein the arrays in a bank are arranged linearly | (claim 7 of Patent 6,662,271) |
| | a plurality of arrays of memory cells, the arrays being arranged in banks, each bank including regular arrays, A.sub.0-N, and a redundant array; |
| | a data bus having sets of N sets of bus lines, B.sub.0-N, for connection to the arrays; |
| | logic associated with each array, the logic being configured with a bit that is set to a first state to connect an ith regular array to an ith set of the bus lines, with the redundant array being disconnected from the data bus; |
| | and a change in the bit setting from the first state to a second state causing the regular array. |
| | A.sub.i, to be disconnected from the data bus and the redundant array to be connected to the data bus, |
| regular arrays, A.sub.0 to A.sub.(i-1) connect to bus lines B.sub.0 to B.sub.(i-1), respectively, | wherein regular arrays, A.sub.0 to A.sub.(i-1) connect to bus lines B.sub.0 to B.sub.(i-1), respectively, |
| and regular arrays, A.sub.(i+1) to A.sub.N connect to bus lines B.sub.i to B.sub.(N-1), | and regular arrays, A.sub.(i+1) to A.sub.N connect to bus lines B.sub.i to B.sub.(N-1), |

| | |
|---|---|
| respectively, responsive to the change | respectively, responsive to the change |

With respect to claim 10, claim 13 of Patent 6,662,271 is identical to claim 10 of the instant application.

With respect to claim 12, claims 16 of Patent 6,662,271 disclose the cache of the instant application. Please refer to the table below, illustrating the anticipatory relationship of the claims:

| **Instant Application** | **Patent 6,662,271** |
|---|---|
| 12. A method of operation for a cache, comprising: | A method comprising: |
| changing a single bit associated with a cache bank from a first to a second logic state, the cache bank comprising a plurality of arrays of memory cells, the arrays including regular arrays, A.sub.0-N, and a redundant array, | changing a single bit associated with a cache bank from a first to a second logic state, the cache bank comprising a plurality of arrays of memory cells, the arrays including regular arrays. A.sub.0-N, and a redundant array, |
| the regular arrays being connected to corresponding bus lines, B.sub.0-N, of a data bus when the single bit is in the first logic state; | the regular arrays being connected to corresponding bus lines, B.sub.0-N, of a data bus when the single bit is in the first logic state; |
| disconnecting a regular array, A.sub.i, from the data bus data bus responsive to the single bit state being changed to the second logic state; | disconnecting a regular array, A.sub.i, from the data bus data bus responsive to the single bit state being changed to the second logic state; |
| connecting the redundant array to the data bus responsive to the single bit state being changed to the second logic state. | connecting the redundant array to the data bus responsive to the single bit state being changed to the second logic state, |
| | wherein regular arrays, A.sub.0 to A.sub.(i-1) connect to bus lines B.sub.0 to B.sub.(i-1), respectively, and regular arrays, A.sub.(i+1) to A.sub.N connect to bus lines B.sub.i to B.sub.(N-1), respectively, responsive to the single bit state being changed to the second logic state. |

With respect to claims 13-14, claims 18-19 of Patent 6,662,271 are identical to claims 13-14 of the instant application.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (703) 305-7850. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Inoa
Examiner
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MI

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8/20/04

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